4. Interface

Hardware manual

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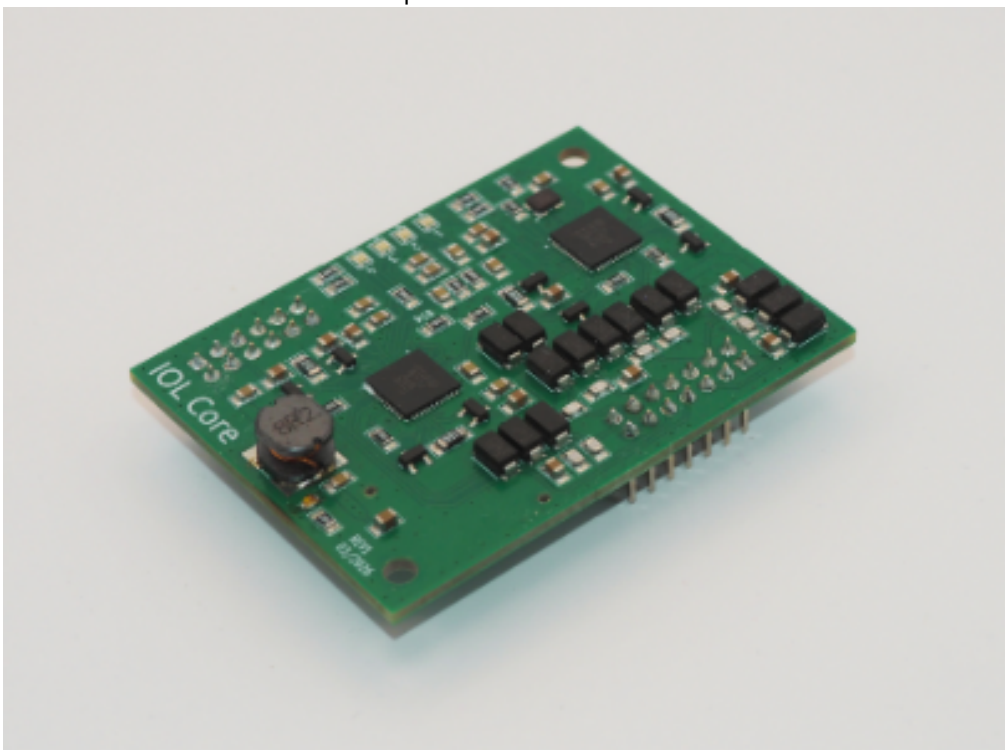


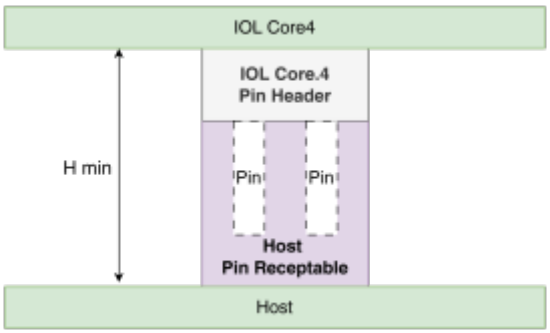
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4. Interface

4.1 General Considerations

- The host connector and IOL connectors are 2,54mm pitch pin header with a pin length of 6mm.
- The clearance under the board shall be min. H=3,5mm.



4.2 Power Supply

- The 24V power supply voltage shall be 24V +/- 20%.
- The host connector shall be able to provide 2A on the 24V supply.
- The voltage is filtered to provide EMC compatibility on the IOL ports when integrated.



Please note that the 24V voltage supply is not reverse polarity protected.

4.3 Host Connector X1

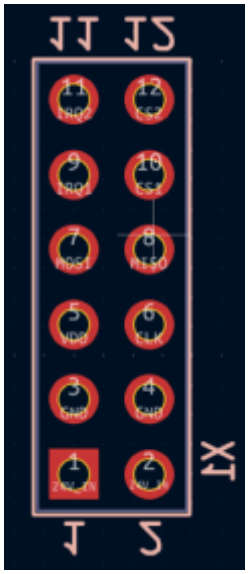
- The Vdd provides a reference level for the logic communication (SPI, IRQ) and supply for the µC on the module (IOL Core4 µC only)
- The Vdd voltage is 3,3V +/- 10%. The maximum current on this line is:
  - IOL Core4 (PT-1204) <20mA.
  - IOL Core4 µC (PT-1205) <75mA.
- The logic communication lines (SPI, IRQ) do not include ESD protection in order to preserve signal integrity. This needs to be considered on the host if the lines are ESD-exposed.

Pin assignment:

Pin	Signal
1,2	24V IN
3,4	GND
5	Vdd, logic reference (3.2V)
6	SPI CLK (logic level)
7	SPI MOSI (logic level)
8	SPI MISO (logic level)
9	IRQ1 (logic level) to MAX1 – has an internal pull-up
10	CS1 (logic level) to MAX1

Pin	Signal
11	IRQ2 (logic level) to MAX2 – has an internal pull-up
12	CS2 (logic level) to MAX2

Host connector X1 TOP view:



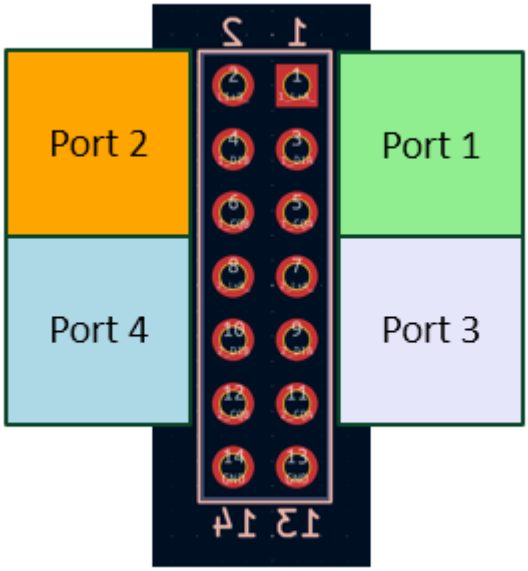
All logic signals (SPI, interrupts) host interface X1 work on 3V3 logic levels.

4.4 IOL Connector

Pin assignment:

Pin	Port	Signal
1	Port 1 (IOL1A)	L+
2	Port 2 (IOL1B)	L+
3	Port 1 (IOL1A)	DIA
4	Port 2 (IOL1B)	DIA
5	Port 1 (IOL1A)	CQB
6	Port 2 (IOL1B)	CQB
7	Port 3 (IOL2A)	L+
8	Port 4 (IOL2B)	L+
9	Port 3 (IOL2A)	DIA
10	Port 4 (IOL2B)	DIA
11	Port 3 (IOL2A)	CQB
12	Port 4 (IOL2B)	CQB
13,14	Common	GND

IOL connector X2 TOP view:



Each SDCI Port is designed to supply max. 500mA on the L+ line and 150mA on the CQ line. The current supply is limited by software (for L+ in connection with a series resistor). If a custom master application is used, the limits must be set in the driver configuration.